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(54) [Title of the Invention] MULTILAYER CERAMIC CAPACITOR FOR BALANCED LINE

(57) [Abstract]

[Object] It is an object of the present invention to provide a small-size multilayer ceramic capacitor which can be mounted with a high density on a circuit substrate with a small mounting area, thereby making it possible to decrease the size of electronic devices, and which can improve the filter response and remove a high-frequency noise.

[Structure] A laminate 45 is formed by alternately laminating a dielectric sheet 10 having formed on its surface an inner electrode 10a which is extended to one outer side and is located at a certain distance from the outer side opposite to the above-mentioned outer side, a dielectric sheet 20 having formed on its surface an inner electrode 20a which is extended to the above-mentioned opposite outer side and is located at a certain distance from the above-mentioned one outer side, and a dielectric sheet 30 having formed on its surface an inner electrode 30a which is extended to the two mutually opposite outer sides, to which electrodes 10a, 20a are not extended, and is located at a certain distance from the two mutually opposite outer sides, to which electrodes 10a, 20a are extended. A pair of outer electrodes 41, 42 which are connected to electrodes 10a, 20a are formed on both side surfaces of the laminate, and outer electrodes 43 connected to electrode 30a are

formed on other two side surfaces of the laminate. Three capacitors are incorporated, and three terminals are integrated.

[Patent Claims]

[Claim 1] A multilayer ceramic capacitor for a balanced line comprising

a laminate (45) formed by alternately laminating

a first rectangular ceramic dielectric sheet (10) having formed on its surface a first inner electrode (10a) which is extended to one outer side and is located at a certain distance from the outer side opposite to the above-mentioned outer side,

a second rectangular ceramic dielectric sheet (20) having formed on its surface a second inner electrode (20a) which is extended to the above-mentioned opposite outer side and is located at a certain distance from the above-mentioned one outer side,

and a third ceramic dielectric sheet (30) having formed on its surface a third inner electrode (30a) which is extended to the two mutually opposite outer sides to which said first and second electrodes (10a, 20a) are not extended and is located at a certain distance from the two mutually opposite outer sides to which said electrodes (10a, 20a) are extended,

a pair of a first and second outer electrodes (41, 42) for connecting a balanced line, which are formed on both side surfaces of said laminate (45) and are connected to said first and second inner electrodes (10a, 20a), and

third outer electrodes (43) for grounding, which are formed on other two side surfaces of said laminate (45) and are connected to said third inner electrode (30a).

[0001]

[Detailed Description of the Invention]

[Field of Industrial Utilization] The present invention relates to a multilayer ceramic capacitor suitable as a chip noise filter for balanced lines of communication circuits such as telephones and modems, or power supply circuits such as DC-DC converters. More specifically, the present invention relates to a chip bypass capacitor suitable for absorbing electromagnetic interference, in which three capacitors are incorporated and three terminals are integrated.

[0002]

[Prior Art Technology] Three wire balanced lines consisting of a pair of input lines and a ground line are suitable for the communication circuits of power supply circuits of the above-described type. Low-pass filters or bypass filters are required to remove a common-mode noise and differential noise in such lines. More specifically, a filter is often used in which, as shown in Fig 17, a multilayer ceramic capacitor C_1 is connected between the input line A and ground line G, a multilayer ceramic capacitor C_2 is connected between the input line B and ground line G, and a multilayer ceramic capacitor C_3 is connected between input lines A and B. Each of the above-mentioned three multilayer ceramic capacitors comprises a laminate and a pair of external electrodes. The

laminate is obtained by preparing two of rectangular ceramic dielectric sheets each having formed on its surface an inner electrode which is extended to one outer side of the sheet and is located at a certain distance from the sheet outer side which is opposite to the above-mentioned sheet outer side, stacking those two ceramic dielectric sheets so that the sheet outer sides with the inner electrodes extended thereto are on respective opposite sides, and laminating and integrating a plurality of such stacked and assembled ceramic dielectric sheets. A pair of outer electrodes is formed so as to be connected to the respective inner electrodes exposed on both side surfaces of the laminate. Those three capacitors are separately mounted on a printed circuit board.

[0003]

[Problems Addressed by the Invention] Thus, in the conventional filters consisting of the above-described three multilayer ceramic capacitors, the capacitors were separately mounted on a substrate. As a result the printed circuit was complex and the noise absorption capability of the filter was degraded due to the residual impedance of the printed circuit. Furthermore, when the capacitor was mounted on a substrate, the substrate was required to have a large mounting area, and the size of electronic devices was difficult to decrease. It is an object of the present invention to provide a small-size, multilayer ceramic capacitor for a balanced line, which can be mounted with a high density on a circuit substrate with a small mounting area, thereby making it possible to decrease the size of electronic devices. Another object of the present invention is to provide a multilayer ceramic capacitor for a balanced line, which makes it possible to improve filter response and to remove a common-mode noise and differential noise in a three-wire balanced line by incorporating three capacitors close to each other in a single element and integrating three terminals.

[0004]

[Means to Resolve the Problems] The structure of the present invention designed to attain the above-described object will be described below with reference to Fig 1, Fig 5, and Fig 8. In a multilayer ceramic capacitor 50 in accordance with the present invention, a laminate 45 is formed by alternately laminating a first rectangular ceramic dielectric sheet 10 having formed on its surface a first inner electrode 10a which is extended to one outer side and is located at a certain distance from the outer side opposite to the above-mentioned outer side, a second rectangular ceramic dielectric sheet 20 having formed on its surface a second inner electrode which is extended to the above-mentioned opposite outer side and is located at a certain distance from the above-mentioned one outer side, and a third ceramic dielectric sheet 30 having formed on its surface a third inner electrode 30a which reaches the two mutually opposite outer sides to which the two electrodes 10a, 20a were not extended and is located at a certain distance from the two mutually opposite outer sides to which the two electrode 10a, 20a were extended. Furthermore, a first and second outer electrodes 41, 42 for a balanced line connection, which are connected to the electrodes 10a, 20a, respectively, are formed on both side surfaces of laminate 45, and third outer electrodes 43 for grounding, which are connected to the third inner electrode 30a, are formed on other two side surfaces of laminate 45.

[0005]

[Operation] As shown in Fig 8, when capacitor 50 is connected to lines A, B, and G, a capacitor C_3 for absorbing a differential noise is formed between the first outer electrode 41 and second outer electrode 42, and two capacitors C_1 and C_2 for absorbing a common-mode noise are formed between the first outer electrode 41 and third outer electrode 43, and between the second outer electrode 42 and third outer electrode 43, respectively. In the chip-like multilayer ceramic capacitor having the above-described structure, the three capacitors are located inside and three terminal electrodes 41, 42, 43 are integrated with side surfaces of laminate 45. Therefore, (1) the filter response is improved, and (2) three capacitors, which are implemented in a single element, take a very small space and can be mounted on a circuit substrate by a process involving few operations.

[0006]

[Embodiments] The embodiments of the present invention will be described below in greater detail with reference to the drawings attached.

<Embodiment 1> First, a large number of dielectric green sheets were prepared. Those dielectric green sheets were formed by coating a barium titanate-based dielectric slurry having a JIS-R characteristic by a doctor blade method on the upper surface of a polyester base sheet, followed by drying. Of those green sheets, a certain group was taken as first green sheets, another group was taken as second green sheets, and still another group was taken as third green sheets. Then, a conductive paste containing Ag/Pd as the main components was screen printed according to respective patterns on the surfaces of the first, second, and third green sheets, followed by drying for 4 min at a temperature of 80°C. Thus, as shown in Fig 5, a first inner electrode 10a was formed by printing on the surface of first green sheets 10 in such a manner that it was extended to one outer side and was located at a certain distance from the outer side opposite to the above-mentioned outer side. A second inner electrode 20a was formed by printing on the surface of second green ceramic green sheets in such a manner that it was extended to the above-mentioned opposite outer side and was located at a certain distance from the above-mentioned one outer side. Then, a cross-like third inner electrode 30a was formed by printing on the surface of third ceramic green sheets in such a manner that it was extended to two mutually opposite outer sides to which the two inner electrodes 10a, 20a were not extended and was located at a certain distance from the two mutually opposite outer sides to which the two inner electrodes 10a, 20a were extended. In this example, the three inner electrodes 10a, 20a, and 30a had the same surface area.

[0007] As shown in Fig 1 and Fig 5, in this example a first dielectric sheet 10, a third dielectric sheet 30, a second dielectric sheet 20, a first dielectric sheet 10, a third dielectric sheet 30, and a second dielectric sheet 20 were laminated on the second dielectric sheet 20 in the order of description. A fourth ceramic green sheet 40 that was not printed with the electrically conductive paste was placed on the uppermost layer to obtain a laminate 45 consisting of a total of 8 layers. This laminate 45 was integrated by

thermal pressing and fired for about 1 h at a temperature of 130°C to obtain a sintered body. The sintered body was barrel polished to expose the inner electrodes 10a, 20a, and 30a on the side surface of the sintered body (Fig 6). Both end portions of the sintered body where the inner electrodes 10a, 20a were exposed were coated with an electrically conductive paste containing Ag as the main component, and then the electrically conductive paste was coated on the whole periphery of the central portion of the sintered body where the inner electrode 30a was exposed. The electrically conductive paste in all of the above-mentioned regions was then fired to form the first and second outer electrodes 41, 42 and a third outer electrode 43. As a result, a multilayer ceramic capacitor 50 shown in Fig 7 was obtained.

[0008] In order to study characteristics of the multilayer ceramic capacitor 50, it was connected to a three-wire balanced line including a pair of input lines A and B and a ground line G (see Fig 8). More specifically, the first outer electrode 41 of the multilayer ceramic capacitor 50 was connected to line A, the second outer electrode 42 was connected to line B, and the third outer electrode 43 was connected to line G. When a signal to which a high-frequency noise, electromagnetic waves and the like were admixed was fed into the balanced line, a differential noise was absorbed between the first outer electrode 41 and second outer electrode 42, and the respective common-mode noise was absorbed between the first outer electrode 41 and third outer electrode 43, and between the second outer electrode 42 and third outer electrode 43. In this example, the capacitance of the three capacitors in the circuit shown in Fig 8 can be represented by the following formula.

$$C_1 = C_2 = C_3 \qquad (1)$$

[0009] <Embodiment 2> Figs 9 – 12 show a cross section of the multilayer ceramic capacitor of the second embodiment of the present invention. In those figures, structural components identical to those shown in Figs 1 – 4 are assigned with the same symbols. In this embodiment, the third dielectric sheet 30, second dielectric sheet 20, third dielectric sheet 30, first dielectric sheet 10, third dielectric sheet 30, and second dielectric sheet 20 were laminated in the order of description on the first dielectric sheet 10. A fourth ceramic green sheet 40 that was not printed with the electrically conductive paste was placed on the uppermost layer to obtain a laminate 45 consisting of a total of 8 layers. In this example, the surface area of inner electrode 30a was half of the surface area of each of the inner electrode 20a and inner electrode 30a. Other elements of the structure were identical to those of Embodiment 1, and their explanation is omitted to avoid redundancy. Characteristics of the multilayer ceramic capacitor were identical to those obtained in Embodiment 1. In this example, the capacitance of the three capacitors in the circuit shown in Fig 8 can be represented by the following formula.

$$C_1 = C_2 = C_3/2.5 \qquad (2)$$

[0010] <Embodiment 3> Figs 13 – 16 show a cross section of the multilayer ceramic capacitor of the third embodiment of the present invention. In those figures, structural components identical to those shown in Figs 1 – 4 are assigned with the same symbols. In

this embodiment, the first dielectric sheet 10, second dielectric sheet 20, third dielectric sheet 30, first dielectric sheet 10, second dielectric sheet 20, first dielectric sheet 10, third dielectric sheet 30, and second dielectric sheet 20 were laminated in the order of description on the second dielectric sheet 20. A fourth ceramic green sheet 40 that was not printed with the electrically conductive paste was placed on the uppermost layer to obtain a laminate 45 consisting of a total of 10 layers. In this example, the surface area of the three inner electrodes 10a, 20a, and 30a was the same. Other elements of the structure were identical to those of Embodiment 1, and their explanation is omitted to avoid redundancy. Characteristics of the multilayer ceramic capacitor were identical to those obtained in Embodiment 1. In this example, the capacitance of the three capacitors in the circuit shown in Fig 8 can be represented by the following formula.

$$C_1 = C_2 = C_3/2 \qquad (3)$$

[0011] Furthermore, the number of layers in the ceramic dielectric sheet in accordance with the present invention and the surface area of the third inner electrode 30a employed for grounding are not limited to the above-described embodiments and can be changed appropriately according to the required capacitance.

[0012]

[Effect of the Invention] As described above, the present invention provided a small capacitor in which three capacitors are incorporated in a single element and three terminals are integrated. As a result, mounting can be conducted by a process consisting of a small number of operations and a printed circuit substrate is not required to have a large mounting area. At the same time, the filter response can be improved. Furthermore, a common-mode noise and differential noise in three-wire balanced lines can be removed. Therefore, the capacitor in accordance with the present invention is suitable as a chip noise filter (CNF) absorbing electromagnetic interference (EMI). Another advantage of the capacitor in accordance with the present invention is that the capacitance of the incorporated capacitors can be changed by changing the surface area of the second inner electrode with respect to the surface area of the first inner electrode.

[Brief Description of the Drawings]

Fig 1 is a cross section along the line H-H in Fig 7 for which the relation $C_1 = C_2 = C_3$ is valid, this relation being obtained for the multilayer ceramic capacitor which is an embodiment of the present invention.

Fig 2 is a cross section along the line J-J relating to the same embodiment.

Fig 3 is a cross section along the line K-K relating to the same embodiment.

Fig 4 is a cross section along the line L-L relating to the same embodiment.

Fig 5 is a perspective view prior to lamination in a laminate preparation.

Fig 6 is a perspective view of a sintered body prepared by sintering the laminate.

Fig 7 is a perspective view of a multilayer ceramic capacitor fabricated by arranging first, second, and third outer electrodes on the sintered body.

Fig 8 is a circuit diagram illustrating connection of the multilayer ceramic capacitor to a balanced line.

Fig 9 is a cross section corresponding to Fig 1 for which the relation $C_1 = C_2 = C_3/2.5$ is valid, this relation being obtained for the multilayer ceramic capacitor which is another embodiment of the present invention.

Fig 10 is a cross section along the line M-M relating to the same embodiment.

Fig 11 is a cross section along the line N-N relating to the same embodiment.

Fig 13 is a cross section along the line O-O relating to the same embodiment.

Fig 9 is a cross section corresponding to Fig 1 for which the relation $C_1 = C_2 = C_3/2$ is valid, this relation being obtained for the multilayer ceramic capacitor which is another embodiment of the present invention.

Fig 14 is a cross section along the line P-P relating to the same embodiment.

Fig 15 is a cross section along the line Q-Q relating to the same embodiment.

Fig 16 is a cross section along the line R-R relating to the same embodiment.

Fig 17 is a circuit diagram illustrating connection of a conventional multilayer ceramic capacitor to a balanced line.

[Legends]

10 – first ceramic dielectric sheet (first ceramic green sheet)
10a – first inner electrode
20 – second ceramic dielectric sheet (second ceramic green sheet)
20a – second inner electrode
30 – third ceramic dielectric sheet (third ceramic green sheet)
30a – third inner electrode
41 – first outer electrode
42 – second outer electrode
43 – third outer electrode
45 – laminate
50 – multilayer ceramic capacitor

Fig 1

10 – first ceramic dielectric sheet (first ceramic green sheet)
10a – first inner electrode
20 – second ceramic dielectric sheet (second ceramic green sheet)
20a – second inner electrode
30 – third ceramic dielectric sheet (third ceramic green sheet)
30a – third inner electrode
41 – first outer electrode
42 – second outer electrode
43 – third outer electrode
50 – multilayer ceramic capacitor

Fig 2
Fig 3

Fig 4

Fig 5
45 – laminate

Fig 6
Fig 7
Fig 8
Fig 9
Fig 10
Fig 11
Fig 12
Fig 13
Fig 14
Fig 15
Fig 16
Fig 17

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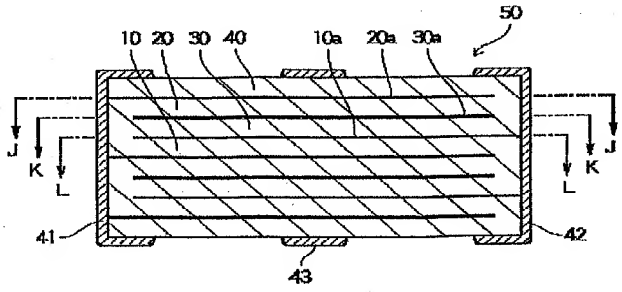
(54)【発明の名称】　平衡線路用積層セラミックコンデンサ

(57)【要約】

【目的】　小型で実装面積が少なくて済み、高密度に回路基板に実装して電子機器を小型化でき、かつフィルタ応答性を改善して、高周波ノイズを除去する。

【構成】　１つの外周辺まで延びこの外周辺と反対側の外周辺とは間隔をあけて内部電極１０ａを表面に形成した誘電体シート１０と、前記反対側の外周辺まで延び前記１つの外周辺とは間隔をあけて内部電極２０ａを表面に形成した誘電体シート２０と、両電極１０ａ，２０ａの延びていない相対向する２つの外周辺まで延び両電極１０ａ，２０ａの延びている相対向する２つの外周辺とは間隔をあけて内部電極３０ａを表面に形成した誘電体シート３０とを交互に積重ねて積層体４５を形成する。積層体の両側面に両電極１０ａ，２０ａに接続する一対の外部電極４１，４２を形成し、積層体の別の両側面に電極３０ａに接続する外部電極４３を形成する。３個のコンデンサが内蔵され３端子が一体化される。



10　第１セラミック誘電体シート(第１セラミックグリーンシート)
10a　第１内部電極
20　第２セラミック誘電体シート(第２セラミックグリーンシート)
20a　第２内部電極
30　第３セラミック誘電体シート(第３セラミックグリーンシート)
30a　第３内部電極
41　第１外部電極
42　第２外部電極
43　第３外部電極
50　積層セラミックコンデンサ

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【特許請求の範囲】

【請求項１】　１つの外周辺まで延びこの外周辺と反対側の外周辺とは間隔をあけて第１内部電極(10a)が表面に形成された角形の第１セラミック誘電体シート(10)と、

前記反対側の外周辺まで延び前記１つの外周辺とは間隔をあけて第２内部電極(20a)が表面に形成された角形の第２セラミック誘電体シート(20)と、

前記第１及び第２内部電極(10a,20a)の延びていない相対向する２つの外周辺まで延び前記第１及び第２内部電極(10a,20a)の延びている相対向する２つの外周辺とは間隔をあけて第３内部電極(30a)が表面に形成された第３セラミック誘電体シート(30)とを交互に積重ねて形成された積層体(45)と、

前記積層体(45)の両側面にそれぞれ形成され前記第１及び第２内部電極(10a,20a)に接続する平衡線路接続用の一対の第１及び第２外部電極(41,42)と、

前記積層体(45)の別の両側面にそれぞれ形成され前記第３内部電極(30a)に接続する接地用の第３外部電極(43)とを備えた平衡線路用積層セラミックコンデンサ。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は電話機、モデム等の通信回路、或いはＤＣ－ＤＣコンバータ等の電源供給回路の平衡線路にチップ型ノイズフィルタ（chip noise filter）として用いられる積層セラミックコンデンサに関する。更に詳しくは３個のコンデンサが内蔵されかつ３端子が一体化された、電磁妨害ノイズ（electromagnetic inter-ference）を吸収するに適したチップ型のバイパスコンデンサに関するものである。

【０００２】

【従来の技術】この種の通信回路又は電源供給回路には、一対の入力線路とアース線路からなる三線の平衡線路（three wire balanced line）が使用される。こうした回路には同相ノイズ（common-mode noise）や差動ノイズ（differential noise）を除去するためにローパスフィルタ又はバイパスフィルタが必要である。具体的には、図１７に示すように入力線路Ａとアース線路Ｇとの間に積層セラミックコンデンサC_1を、入力線路Ｂとアース線路Ｇとの間に積層セラミックコンデンサC_2を、また入力線路ＡとＢの間に積層セラミックコンデンサC_3をそれぞれ接続したフィルタがしばしば用いられる。従来、上記３個の積層セラミックコンデンサのそれぞれは、１つのシート外周辺まで延びこのシート外周辺と反対側のシート外周辺とは間隔をあけてシート表面に内部電極が形成された角形の２枚のセラミック誘電体シートを一組とし、これら２枚のセラミック誘電体シートを内部電極の延びたシート外周辺がそれぞれ反対側になるように重ね合せ、この重ね合せた一組のセラミック誘電体シートを複数組積層し一体化してなる積層体と、積層体

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の両側面にそれぞれ露出した内部電極に接続して形成された一対の外部電極とを備える。そして３個のコンデンサはプリント回路基板に別々に実装される。

【０００３】

【発明が解決しようとする課題】このため、従来の３個の積層セラミックコンデンサからなるフィルタでは、個別にコンデンサを基板に実装するため、プリント配線が複雑になり、プリント配線の残留インダクタンスのため、フィルタとしてのノイズ吸収性能に劣っていた。更にコンデンサを基板に実装する際に、基板に広い実装面積を必要とし、電子機器を小型化できない問題点があった。本発明の目的は、小型で実装面積が少なくて済み、高密度に回路基板に実装して電子機器を小型化できる平衡線路用積層セラミックコンデンサを提供することにある。本発明の別の目的は、単一の素子で３個のコンデンサを近接して内蔵しかつ３端子を一体化することにより、フィルタ応答性が改善された、三線の平衡線路における同相ノイズや差動ノイズの除去が可能な平衡線路用積層セラミックコンデンサを提供することにある。

【０００４】

【課題を解決するための手段】上記目的を達成するための本発明の構成を図１、図５及び図８に基づいて説明する。本発明の積層セラミックコンデンサ５０は、１つの外周辺まで延びこの外周辺と反対側の外周辺とは間隔をあけて第１内部電極１０ａが表面に形成された角形の第１セラミック誘電体シート１０と、前記反対側の外周辺まで延び前記１つの外周辺とは間隔をあけて第２内部電極２０ａが表面に形成された角形の第２セラミック誘電体シート２０と、両電極１０ａ，２０ａの延びていない相対向する２つの外周辺まで延び両電極１０ａ，２０ａの延びている相対向する２つの外周辺とは間隔をあけて第３内部電極３０ａが表面に形成された第３セラミック誘電体シート３０とを交互に積重ねて積層体４５が形成される。更に、この積層体４５の両側面には両電極１０ａ，２０ａに接続する平衡線路接続用の一対の第１及び第２外部電極４１，４２がそれぞれ形成され、この積層体４５の別の両側面には第３内部電極３０ａに接続する接地用の第３外部電極４３がそれぞれ形成される。

【０００５】

【作用】図８に示すように、コンデンサ５０を線路Ａ，Ｂ，Ｇに接続すると、第１外部電極４１と第２外部電極４２との間で差動ノイズを吸収するための１つのコンデンサC_3が形成され、第１外部電極４１と第３外部電極４３との間及び第２外部電極４２と第３外部電極４３との間でそれぞれ同相ノイズを吸収するための２つのコンデンサC_1及びC_2が形成される。このような構成のチップ型の積層セラミックコンデンサは、３個のコンデンサが内蔵されかつ３つの端子電極４１，４２，４３が積層体４５の側面に一体化するので、第一にフィルタ応答性が改善され、第二に３個のコンデンサを単一の素子の形

態で、僅かなスペースと僅かな工数で回路基板に実装することができる。

【０００６】

【実施例】次に、本発明の実施例を図面に基づいて詳しく説明する。

＜実施例１＞先ず、誘電体グリーンシートを多数枚用意した。この誘電体グリーンシートはポリエステルベースシートの上面にチタン酸バリウム系のＪＩＳ－Ｒ特性を有する誘電体スラリーをドクターブレード法によりコーティングした後、乾燥して形成される。これらのグリーンシートのうち、ある１群を第１セラミックグリーンシートとし、別の群を第２セラミックグリーンシートとし、更に別の群を第３セラミックグリーンシートとした。次いで第１、第２及び第３セラミックグリーンシートの各表面にそれぞれ別々のパターンでＡｇ／Ｐｄを主成分とする導電性ペーストをスクリーン印刷し、８０℃で４分間乾燥した。即ち、図５に示すように第１セラミックグリーンシート１０の表面には、１つの外周辺まで延びこの外周辺と反対側の外周辺とは間隔をあけて第１内部電極１０ａが印刷形成された。また第２セラミックグリーンシート２０の表面には、前記反対側の外周辺まで延び前記１つの外周辺とは間隔をあけて第２内部電極２０ａが印刷形成された。更に第３セラミックグリーンシート３０の表面には、両内部電極１０ａ，２０ａの延びていない相対向する２つの外周辺まで延び両内部電極１０ａ，２０ａの延びている相対向する２つの外周辺とは間隔をあけて十字状の第３内部電極３０ａが印刷形成された。この例では、３つの内部電極１０ａと２０ａと３０ａの各面積はそれぞれ等しい。

【０００７】図１及び図５に示すように、この例では第２誘電体シート２０の上に、第１誘電体シート１０、第３誘電体シート３０、第２誘電体シート２０、第１誘電体シート１０、第３誘電体シート３０、及び第２誘電体シート２０をこの順に積層した。この最上層には導電性ペーストを全く印刷していない第４セラミックグリーンシート４０を重ね合わせて合計８層の積層体４５を得た。この積層体４５を熱圧着して一体化した後、１３００℃で約１時間焼成して焼結体を得た。この焼結体をバレル研磨して焼結体の周囲側面に内部電極１０ａ，２０ａ及び３０ａを露出させた（図６）。この内部電極１０ａ，２０ａが露出する焼結体の両端部にそれぞれＡｇを主成分とする導電性ペーストを塗布し、また内部電極３０ａが露出する焼結体の中央部の全周に同じ導電性ペーストを塗布した後、これらの導電性ペーストを焼付けて一対の第１及び第２外部電極４１，４２と第３外部電極４３をそれぞれ形成した。これにより、図７に示す積層セラミックコンデンサ５０が得られた。

【０００８】この積層セラミックコンデンサ５０の特性を調べるために、図８に示すように一対の入力線路Ａ及びＢとアース線路Ｇのある三線の平衡線路にこの積層セラミックコンデンサ５０を接続した。具体的には積層セラミックコンデンサ５０の第１外部電極４１を線路Ａに、第２外部電極４２を線路Ｂに、第３外部電極４３を線路Ｇにそれぞれ接続した。この平衡線路に高周波ノイズ、電磁波等を混入した信号を流したところ、第１外部電極４１と第２外部電極４２との間で差動ノイズが吸収され、第１外部電極４１と第３外部電極４３との間及び第２外部電極４２と第３外部電極４３との間でそれぞれ同相ノイズが吸収された。この例では図８の回路において、３つのコンデンサのキャパシタンスは次式で表わされる。

$$C_1 = C_2 = C_3 \quad (1)$$

【０００９】＜実施例２＞図９～図１２は本発明の実施例２の積層セラミックコンデンサの断面図である。これらの図において、図１～図４に示した符号と同一符号は同じ構成部品を示す。この例では第１誘電体シート１０の上に、第３誘電体シート３０、第２誘電体シート２０、第３誘電体シート３０、第１誘電体シート１０、第３誘電体シート３０、及び第２誘電体シート２０をこの順に積層した。この最上層には導電性ペーストを全く印刷していない第４セラミックグリーンシート４０を重ね合わせて合計８層の積層体４５を得た。この例では、内部電極３０ａの面積は内部電極２０ａと３０ａの各面積の半分である。その他の構成は実施例１と同じであるので、繰返しの説明を省略する。この積層セラミックコンデンサの特性は、実施例１と同様であった。ただし、この例では図８の回路において、３つのコンデンサのキャパシタンスは次式で表わされる。

$$C_1 = C_2 = C_3/2.5 \quad (2)$$

【００１０】＜実施例３＞図１３～図１６は本発明の実施例３の積層セラミックコンデンサの断面図である。これらの図において、図１～図４に示した符号と同一符号は同じ構成部品を示す。この例では第２誘電体シート２０の上に、第１誘電体シート１０、第２誘電体シート２０、第３誘電体シート３０、第１誘電体シート１０、第２誘電体シート２０、第１誘電体シート１０、第３誘電体シート３０、及び第２誘電体シート２０をこの順に積層した。この最上層には導電性ペーストを全く印刷していない第４セラミックグリーンシート４０を重ね合わせて合計１０層の積層体４５を得た。この例では、３つの内部電極１０ａと２０ａと３０ａの各面積はそれぞれ等しい。その他の構成は実施例１と同じであるので、繰返しの説明を省略する。この積層セラミックコンデンサの特性は、実施例１と同様であった。ただし、この例では図８の回路において、３つのコンデンサのキャパシタンスは次式で表わされる。

$$C_1 = C_2 = C_3/2 \quad (3)$$

【００１１】なお、本発明のセラミック誘電体シートの積層数、接地用の第３内部電極３０ａの面積の広さは上記例に限られるものではなく、必要とされるキャパシタ

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ンスに応じて適宜変更することができる。

【００１２】

【発明の効果】以上述べたように、本発明によれば、単一の素子で３個のコンデンサを内蔵しかつ３端子を一体化した小型のコンデンサを実現したので、プリント回路基板への実装面積を広く必要とせず、僅かな工数で実装でき、同時にフィルタ応答性を改善できる。また、三線の平衡線路における同相ノイズや差動ノイズの除去することができ、電磁妨害雑音（ＥＭＩ）を吸収するチップ型ノイズフィルタ（ＣＮＦ）として好適に利用できる。更に、第１内部電極の面積に対して第２内部電極の面積を可変にすれば、内蔵するコンデンサのキャパシタンスを変更できる利点もある。

【図面の簡単な説明】

【図１】本発明実施例の積層セラミックコンデンサの$C_1=C_2=C_3$の関係が成立する図７のＨ－Ｈ線断面図。

【図２】そのＪ－Ｊ線断面図。

【図３】そのＫ－Ｋ線断面図。

【図４】そのＬ－Ｌ線断面図。

【図５】その積層体の積層前の斜視図。

【図６】その積層体を焼成した焼結体の斜視図。

【図７】その焼結体に第１～第３外部電極を設けて作製された積層セラミックコンデンサの斜視図。

【図８】その積層セラミックコンデンサを平衡線路に接続した回路図。

【図９】本発明別の実施例の積層セラミックコンデンサの$C_1=C_2=C_3/2.5$の関係が成立する図１に対応

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する断面図。

【図１０】そのＭ－Ｍ線断面図。

【図１１】そのＮ－Ｎ線断面図。

【図１２】そのＯ－Ｏ線断面図。

【図１３】本発明別の実施例の積層セラミックコンデンサの$C_1=C_2=C_3/2$の関係が成立する図１に対応する断面図。

【図１４】そのＰ－Ｐ線断面図。

【図１５】そのＱ－Ｑ線断面図。

【図１６】そのＲ－Ｒ線断面図。

【図１７】従来の積層セラミックコンデンサを平衡線路に接続した回路図。

【符号の説明】

１０　第１セラミック誘電体シート（第１セラミックグリーンシート）

１０ａ　第１内部電極

２０　第２セラミック誘電体シート（第２セラミックグリーンシート）

２０ａ　第２内部電極

３０　第３セラミック誘電体シート（第３セラミックグリーンシート）

３０ａ　第３内部電極

４１　第１外部電極

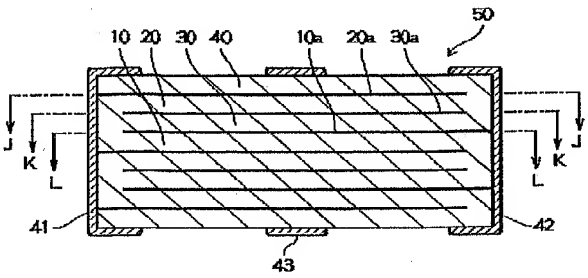
４２　第２外部電極

４３　第３外部電極

４５　積層体

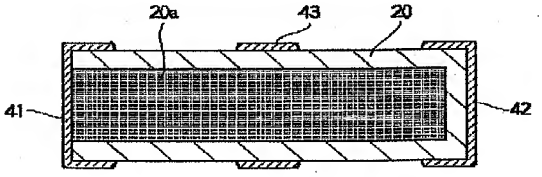
５０　積層セラミックコンデンサ

【図１】

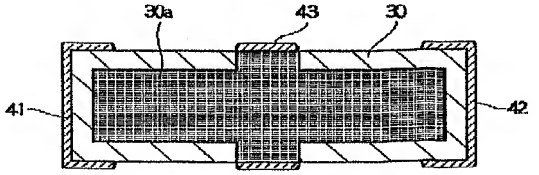


10　第１セラミック誘電体シート（第１セラミックグリーンシート）
10a　第１内部電極
20　第２セラミック誘電体シート（第２セラミックグリーンシート）
20a　第２内部電極
30　第３セラミック誘電体シート（第３セラミックグリーンシート）
30a　第３内部電極
41　第１外部電極
42　第２外部電極
43　第３外部電極
50　積層セラミックコンデンサ

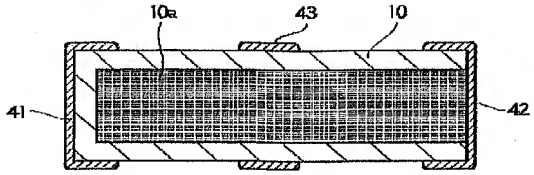
【図２】



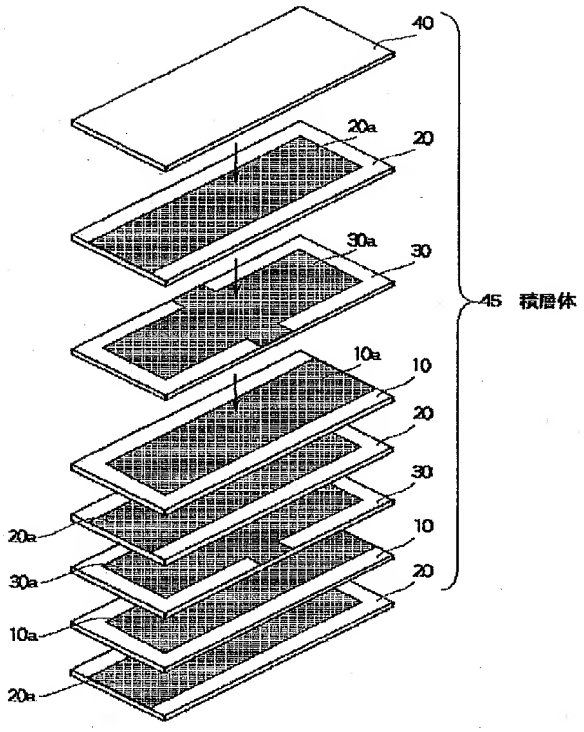
【図３】



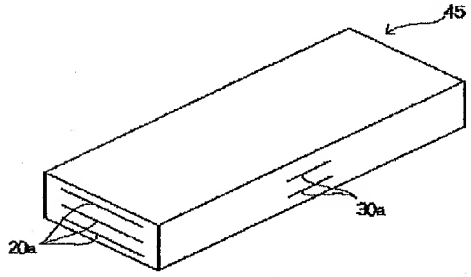
【図4】



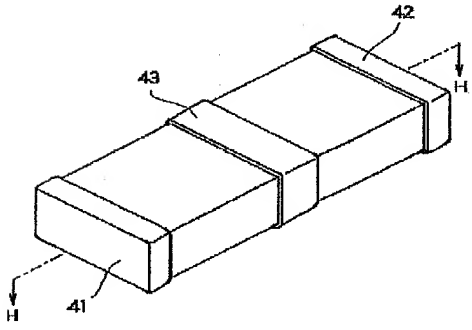
【図5】



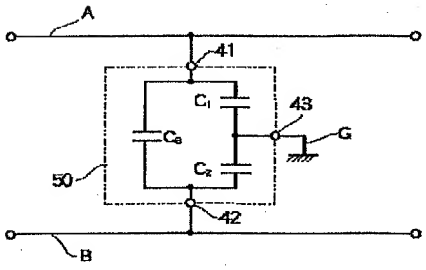
【図6】



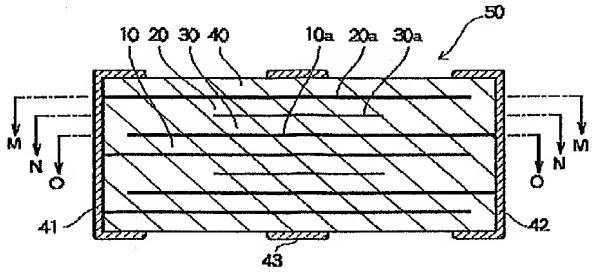
【図7】



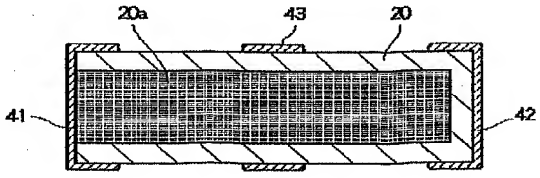
【図8】



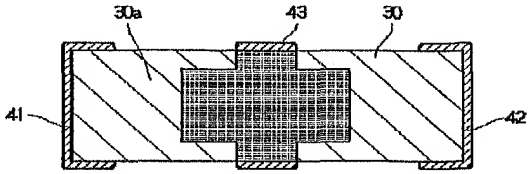
【図9】



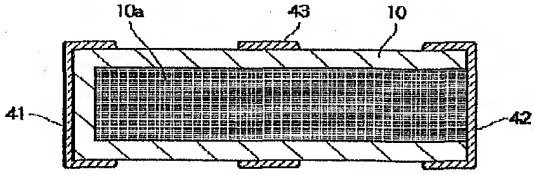
【図10】



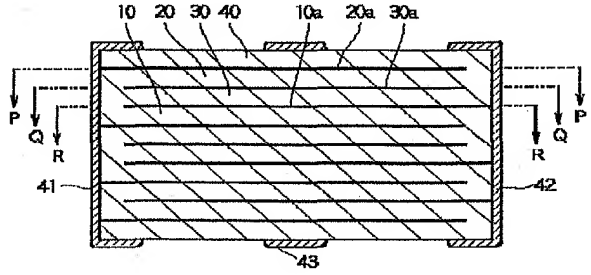
【図１１】



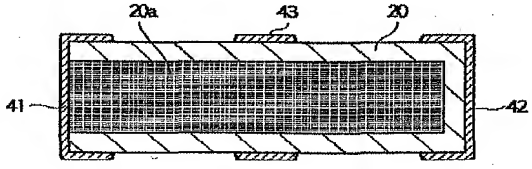
【図１２】



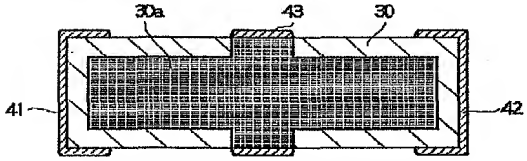
【図１３】



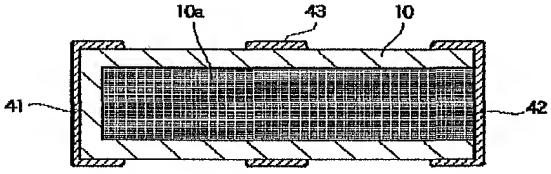
【図１４】



【図１５】



【図１６】



【図１７】